

# Arm® TBSAv8-M Architecture Test

Revision: r0p0

## **Validation Methodology and User Guide**



# Arm® TBSAv8-M Architecture Test

## Validation Methodology and User Guide

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### Release Information

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The information in this document is for a Beta product, that is a product under development.

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# Preface

This preface introduces the *Arm® TBSAv8-M Architecture Test Validation Methodology and User Guide*.

It contains the following:

- *About this book* on page 7.
- *Feedback* on page 9.

## About this book

This book describes the TBSAv8-M Architecture Test Validation Methodology.

### Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

*rm* Identifies the major revision of the product, for example, r1.

*pn* Identifies the minor revision or modification status of the product, for example, p2.

### Intended audience

This user guide is written for engineers who are validating an implementation of the Trusted Base System Architecture Test Suites for Armv8-M.

### Using this book

This book is organized into the following chapters:

#### Chapter 1 Introduction

Read this chapter for an introduction to the features and components of the *Trusted Base System Architecture* (TBSA) test suites for Armv8-M.

#### Chapter 2 Porting steps

Read this chapter for information on configuring the test suite.

#### Chapter 3 Architecture test suite

Read this chapter for information on the tests that are provided with the test suite.

#### Appendix A Revisions

This appendix describes the technical changes between released issues of this book.

## Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

## Typographic conventions

### *italic*

Introduces special terminology, denotes cross-references, and citations.

### **bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

### `monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

### monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

### `monospace italic`

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

### `monospace bold`

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments.  
For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

## Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

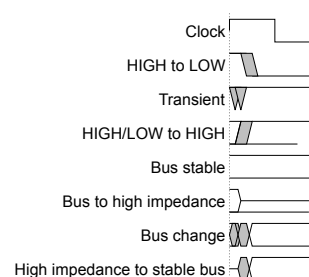


Figure 1 Key to timing diagram conventions

## Signals

The signal conventions are:

### Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.  
Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

### Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

## Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

### Arm publications

- *Arm® Platform Security Architecture Trusted Base System Architecture for Armv8-M* version Beta-1 () DEN 0062A.
- *Arm®v8-M Architecture Reference Manual* (ARM DDI 00553A.b).

### Other publications

None.



## Feedback

### Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

### Feedback on content

If you have comments on content then send an e-mail to [support-psa-arch-tests@arm.com](mailto:support-psa-arch-tests@arm.com). Give:

- The title *Arm TBSAv8-M Architecture Test Validation Methodology and User Guide*.
- The number 101308\_0000\_03\_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

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# Chapter 1

## Introduction

Read this chapter for an introduction to the features and components of the *Trusted Base System Architecture* (TBSA) test suites for Armv8-M.

It contains the following sections:

- [1.1 Abbreviations](#) on page 1-11.
- [1.2 TBSA-v8M test suite](#) on page 1-12.
- [1.3 Components of the test suite](#) on page 1-13.
- [1.4 Compliance sign-off process](#) on page 1-14.
- [1.5 Getting started](#) on page 1-15.
- [1.6 Feedback, contributions, and support](#) on page 1-17.

## 1.1 Abbreviations

This section lists the acronyms that are used in this document.

**Table 1-1 Abbreviations and expansions**

<b>Abbreviation</b>	<b>Expansion</b>
DPM	Debug Protection Mechanism
IDAU	Implementation Defined Attribution Unit
MPU	Memory Protection Unit
NSC	Non-Secure Callable
NVM	Non-Volatile Memory
OTP	One-Time Programmable
PAL	Platform Abstraction Layer
PE	Processing Element
SAU	Security Attribution Unit
TBSA	Trusted Base System Architecture
VAL	Validation Abstraction Layer

## 1.2 TBSA-v8M test suite

The TBSAv8-M test suite checks whether an implementation conforms to the behaviors described in the TBSA specification.

The TBSA-v8M that is described in the TBSA-v8M specification defines the behavior of an abstract machine, referred to as a TBSA-v8M system. Implementations compliant with TBSA-v8M architecture must conform to the described behavior of the TBSA-v8M system.

This test suite includes the following examples:

1. Invariant behaviors that are provided by the TBSA-v8M architecture specification. You can use these examples to verify if these behaviors are interpreted correctly.
2. Areas of the architecture that are fundamental, known pitfalls, and common misinterpretations. The tests are not exhaustive and implementers are responsible for device verification.

The test suite contains basic and assisted architecture tests. System designers building a basic implementation of TBSA-v8M architecture must show compliance using the basic architecture test suites. System designers building an assisted implementation of TBSA-v8M must show compliance using both the basic and assisted architecture test suites.

The test suites contain self-checking tests. The tests are coded in assembly and C, and have checks that are embedded within the source code.

To facilitate test reporting and management of observing aspects, the TBSA-v8M system must contain at least one UART for printing the status of tests.

This section contains the following subsection:

- [1.2.1 Scope of the document on page 1-12.](#)

### 1.2.1 Scope of the document

This document describes the usage of TBSA-v8M test suite and its layers. This document is intended to solicit feedback from partners so that TBSA-v8M test suite can be used agnostic to various system implementations.

Since the TBSA-v8M test suite is at beta stage, only a subset of tests that are released with this suite are validated in the Arm internal platform. Though certain tests have complete source code for a particular scenario, they cannot be validated in the Arm internal platform.

## 1.3 Components of the test suite

The test suite consists of the following components:

Components	Description
Suites	The suites are organized to align with the features of the TBSA-v8M architecture. These suites contain self-checking tests that are written in C language.
Substructure	Test supporting layers consist of a framework and libraries setup as: <ul style="list-style-type: none"><li>• Scripts to build the test suites</li><li>• VAL library</li><li>• PAL library</li></ul>
Documentation	Kit-specific documents.

## 1.4 Compliance sign-off process

Details about the compliance sign-off or certification process, and expectations from partner for this process will be published in the upcoming releases of this document.

## 1.5 Getting started

This section provides the directory structure of the test suite, and the tools and environment requirements for running the test suite.

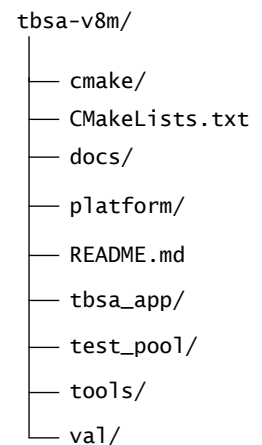
This section contains the following subsections:

- [1.5.1 Directory structure on page 1-15.](#)
- [1.5.2 Software, tools, and licensing requirements on page 1-16.](#)
- [1.5.3 Environment requirements on page 1-16.](#)

### 1.5.1 Directory structure

Validation tests require the components of the test suite to be in a specific hierarchy.

When the test suite release package is downloaded from GitHub, the top-level directory contains the files that are shown in this figure.



**Figure 1-1 Test suite directory structure**

<b>cmake</b>	contains the supporting files for the CMake build.
<b>CMakeLists.txt</b>	CMake build script for TBSAv8-M.
<b>docs</b>	contains the test suite documentation.
<b>platform</b>	contains files to form PAL. PAL is the closest to hardware and is aware of the underlying hardware details. Since this layer interacts with hardware, it is ported or tailored to specific hardware required for system components present in a platform. This layer is also responsible for presenting a consistent interface to the validation abstraction layer required for the tests.
<b>tbsa_app</b>	contains the entry point for TBSA-v8M test suites. It is expected from partner that the SUT boot software would give control to the TBSA-v8M test suite application entry point in the Secure privileged mode.
<b>test_pool</b>	contains the test suites. This test suite is a set of C-based directed tests, each of which verifies the implementation against a test scenario that is described by the TBSA-v8M specification. These tests are abstracted from the underlying hardware platform by the VAL.
<b>tools</b>	contains subdirectories for the tools and scripts that are used in the test suite.
<b>val</b>	contains subdirectories for the VAL libraries. This layer provides a uniform and consistent view of the available test infrastructure to the tests in the test pool. The VAL makes appropriate calls to the PAL to achieve this functionality. This layer is not ported when the underlying hardware changes.

## 1.5.2 Software, tools, and licensing requirements

The test suite requires specific software versions to operate. This list provides the details of the platform and tools that are needed for the test suite.

- Host Operating System: Ubuntu 16.04.4, Windows 10
- Scripting tools: Python3 3
- Other open-source tools: GNUARM 6.3.1, GCC 5.4.0 (Linux Host), mingw 6.3.0 (Windows Host), CMake 3.10

TBSA-v8M test suite is distributed under Apache v2.0 license.

## 1.5.3 Environment requirements

These are the minimum memory requirements for TBSA-v8M test suite to run.

- 32KB of Secure memory and 16KB of Non-secure memory to store VAL or PAL functions and related data
- 16KB of Secure Contiguous Memory for secure tests
- 16KB of Non-secure Contiguous Memory for Non-secure tests
- 8KB of NSC memory

This memory must be usable for both code execution and data access.

---

### Note

- There is no specific requirement on the number of MPU and SAU regions for TBSA-v8M test suites.
  - For Non-secure and NSC memory, it is assumed that SAU or IDAU regions are programmed correctly with Non-secure and Non-secure Callable attributes respectively before getting into `tbsa_entry` point.
- 

The validation tests read the `tbsa_tgt.cfg` file to learn the details of your hardware environment. Refer to [Chapter 2 Porting steps on page 2-18](#).



## 1.6 Feedback, contributions, and support

For feedback, use the GitHub Issue Tracker that is associated with this repository.

For support, send an email to [support-psa-arch-tests@arm.com](mailto:support-psa-arch-tests@arm.com) with the details.

Arm licensees can contact Arm directly through their partner managers. Arm welcomes code contributions through GitHub pull requests. See GitHub documentation on how to raise pull requests.

## Chapter 2

# Porting steps

Read this chapter for information on configuring the test suite.

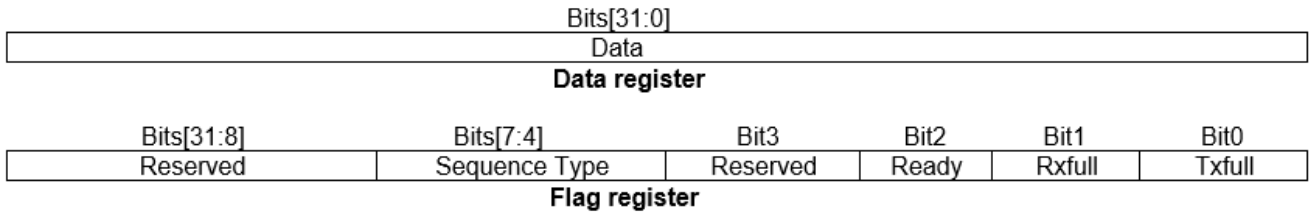
It contains the following section:

- [2.1 Prerequisites for running DPM-related tests in the test suite](#) on page 2-19.

## 2.1 Prerequisites for running DPM-related tests in the test suite

An external debugger is required since *Debug Protection Mechanism* (DPM) scenarios in TBSA-v8M involve verifying whether debug access is allowed in a target or not, based on the DPM settings.

The handshaking and data transfer protocol between the external debugger and the processing element is handled by two memory-mapped registers: data and flag registers. The description of these registers is given in the following table.



**Figure 2-1 Data and flag registers**

**Table 2-1 Bitfield and description**

Bitfield	Description
Txfull	This bit is set when CPU writes to Data register. This bit is cleared when debugger reads the data from Data register.
Rxfull	This bit is set when debugger writes to the data register and cleared when the CPU reads the Data register.
Ready	When this bit is set, the debugger is ready to receive commands (Data).
Sequence Type	This field indicates the appropriate choice of sequence for the debugger depending on what the test expects.

### Note

- The memory-mapped address for these two registers must be chosen in such a way that debug accesses to these addresses are allowed even when Invasive Debug is not allowed. The address for these two registers must be populated in `syscomp_tbsa_m/boards/<platform_name>/tbsa_tgt.cfg`.
- A reference program for DS-5 external debugger is available at `syscomp_tbsa_m/tools/debug/debugger_script.py`. If you use your specific debugger, then you must port this program to use in your debugger-specific commands.

# Chapter 3

## Architecture test suite

Read this chapter for information on the tests that are provided with the test suite.

It contains the following sections:

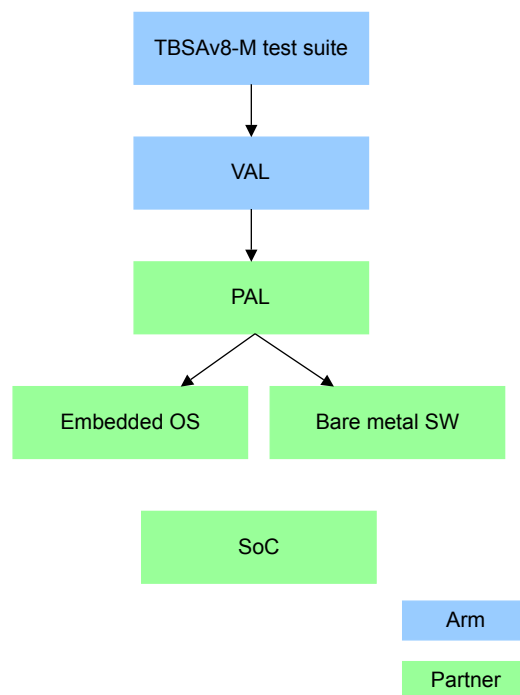
- [3.1 Test layering details on page 3-21.](#)
- [3.2 Build flow on page 3-22.](#)
- [3.3 Test execution flow on page 3-23.](#)
- [3.4 Test dispatcher on page 3-25.](#)
- [3.5 Test naming conventions on page 3-27.](#)
- [3.6 Test status reporting on page 3-28.](#)

### 3.1 Test layering details

The TBSA-v8M tests are self-checking, portable C-based tests with directed stimulus.

These tests use the layered software-stack approach to enable porting across different test platforms. The constituents of the layered stack are:

1. Test suite
2. VAL
3. PAL



**Figure 3-1 Layered software stack**

This table describes the different layers of the test.

**Table 3-1 Test layers and descriptions**

Layer	Description
Test suite	Collection of targeted tests that validate the compliance of the target system. These tests use interfaces that are provided by the VAL.
VAL	Contains subdirectories for the VAL libraries. This layer provides a uniform and consistent view of the available test infrastructure to the tests in the test pool. The VAL makes appropriate calls to the PAL to achieve this functionality. This layer is not ported when the underlying hardware changes.
PAL	This layer is the closest to hardware and is aware of underlying hardware details. Since it interacts with hardware, it must be ported or tailored to specific hardware required for system components present in a platform. It is also responsible for presenting a consistent interface to the validation abstraction layer required for the tests.

## 3.2 Build flow

Each test file must have a metadata section that describes the high-level details of the test such as Test ID, test name, and secure specification requirement. The metadata is filled in the form of macros.

As a precompile step, the metadata in each file is extracted, parsed, and saved in a separate file. The metadata file is used during the package creation phase to fill the `tbsa_test_hdr`. VAL and PAL files are not required to have a metadata section.

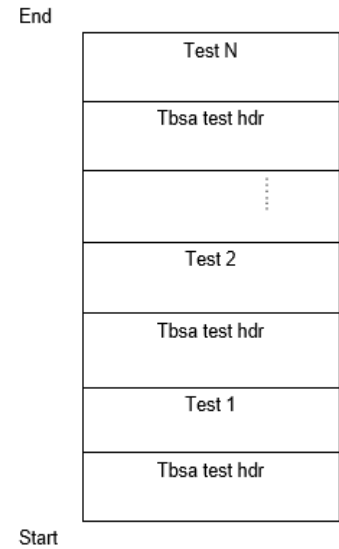


Figure 3-2 Build flow

### Build steps

To compile and build the test images for the complete test suite, use this command:

```
mkdir <build_dir_name>
cd <build_dir_name>
cmake ../-G"Unix Makefiles" -DTARGET=<target_directory_name>
cmake --build .
```

For example,

```
mkdir <build_dir_name>
cd <build_dir_name>
cmake ../-G"Unix Makefiles" -DTARGET=fvp
cmake --build .
```

### Build outputs

The output of the build process is a collection of tests along with metadata of each test packaged as a single binary file: `tbsa_test_combined.bin` and an ELF file: `tbsa.elf`. These files are available in `./<build_dir_name>`

This figure shows the directory structure after building the test ELF images.

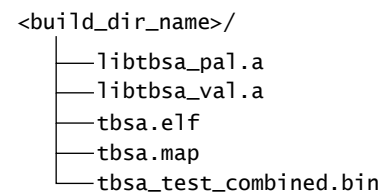
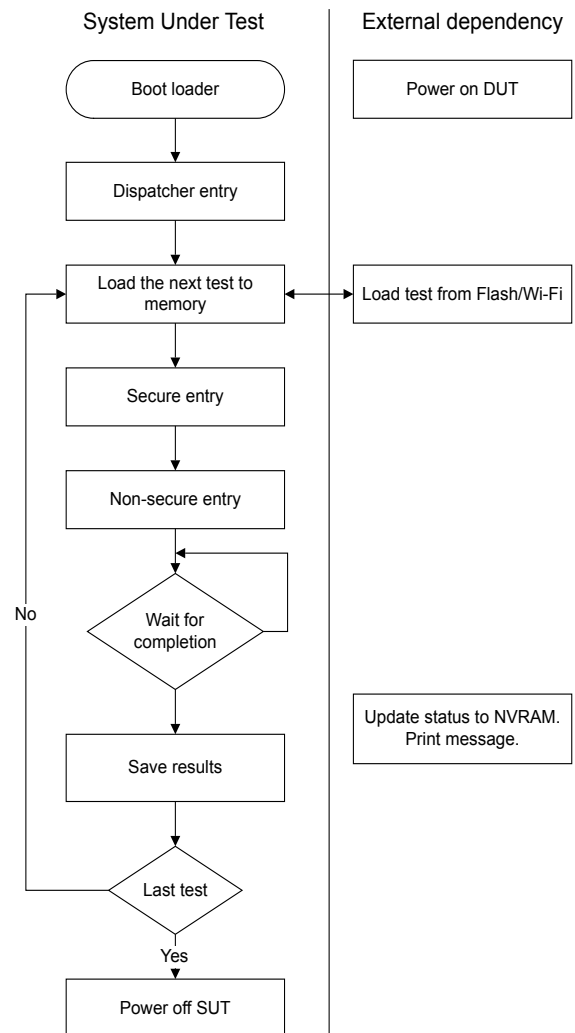


Figure 3-3 TBSA test suite directory structure

### 3.3 Test execution flow

This section describes the test execution flow.



**Figure 3-4 Test execution flow**

1. The SUT boots to an environment that enables the PAL functionality. At this point, the SUT boot software gives control to the TBSA-v8M test suite application entry point `tbsa_entry` that comes from the ELF header of the `tbsa.elf` image in Secure privileged mode.
2. The TBSA-v8M test suite application queries the VAL layer to get the necessary information to run the tests. This information includes memory maps, interrupt maps, and hardware controller maps.
3. Due to RAM and flash size constraints, all the tests may not be available at the same time. The dispatcher in the VAL queries the PAL to load the next test on the completion of the present test. The PAL may optionally communicate with the external world to load the next test. Also, the dispatcher makes VAL (and in turn PAL) calls to save and report each of the test results.
4. Each test must present Secure and Non-secure entry points. If a scenario does not warrant either Secure or Non-secure functionality, then the entry functions are empty.
5. To achieve some of the aforementioned functions, the PAL may optionally make calls that are handled outside the SUT. The following are some of the responsibilities that require external support:
  - Feed the tests to the Design Under Test.
  - Collate and print the test status and messages.
6. Power on/off the system as required by the test sequence. The environment in which a host test harness is running is beyond the scope of this document. But, it is envisioned that the SUT is

communicating with the host using serial port, JTAG, Wi-Fi, USB, or any other means that allow for access to the external world.



## 3.4 Test dispatcher

Each test must present the following test entry points to the dispatcher.

1. Secure
  - a. Entry hook
  - b. Payload
  - c. Exit hook
2. Non-secure
  - a. Entry hook
  - b. Payload
  - c. Exit hook

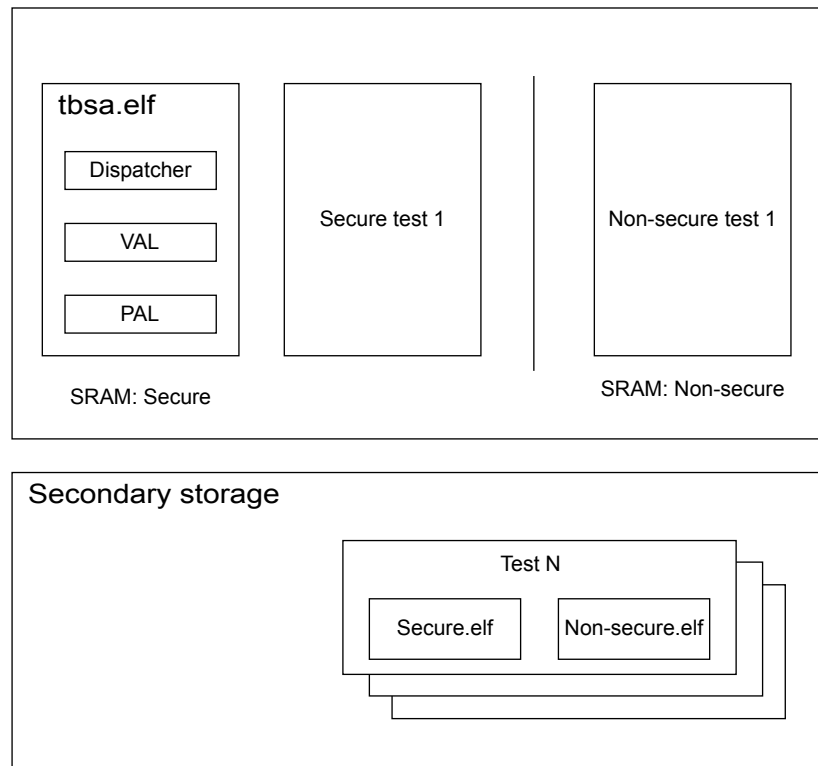
To each of the entry points, the dispatcher passes a pointer to a structure containing the function pointers to all the available VAL functions. The Secure entry points receive the function pointers to the Secure VAL APIs. The Non-secure entry points receive function pointers to the Non-secure wrapper functions in the NSC region. These functions make the appropriate secure VAL function call.

The dispatcher first makes the Secure function calls and on success, calls the Non-secure functions.

The flow of the dispatcher is described in the following steps.

1. Request VAL to load the metadata of the next test into the main memory.
2. Parse the metadata that is associated with the test.
3. Verify that test is compatible with the system under test.
4. Load the test code and data sections to the appropriate locations in the main memory.
5. Call the Secure entry hook function of the test.
6. Call the Secure payload test function.
7. Call the Secure exit hook.
8. Call the Non-secure entry hook function.
9. Call the Non-secure payload function.
10. Call the Non-secure exit hook function.
11. Signal test completion and log test status.

The results from execution of each test are saved to memory. If a display console is not available, the PAL must make available the test results to the external world through other means.



**Figure 3-5 Loading a test from secondary storage**

The `tbsa.elf` is loaded by the bootloader or embedded OS to the Secure memory. The dispatcher within the `tbsa.elf` loads each of the Secure test section to Secure memory and Non-secure test section to Non-secure memory. The addresses of the various sections are predetermined for a given platform as defined by the user and vary for different targets.

## 3.5 Test naming conventions

TBSA-v8M tests are named based on the components as defined in the following table.

**Table 3-2 Test naming conventions**

Component name	Component number	Test number range
Base	0	1-19
Boot	1	21-39
Crypto	2	41-59
Debug	3	61-79
EIP	4	81-99
Interrupts	5	101-119
Secure RAM	6	121-139
Peripherals	7	141-159
Trusted timers	8	161-179
Version counters	9	181-199

Each component can have a maximum of 19 tests, so the test numbers are incremented from their respective base values.

For example, if you see a display as shown below, then for the **Secure RAM**, the component base value is 120. The test name reports it as 121, which means that it is the first test in the **Secure RAM** component.

```
----- Secure RAM Tests -----
121 : "R160/R180_TBSA_INFRA"
```

## 3.6 Test status reporting

When the test suite is run on a target platform, each successfully run test of the suite must report either PASS or SKIP.

The following is a snippet of a successful pass test on the display console.

```

----- Secure RAM Tests -----
121 : "R160/R180_TB_SA_INFRA"
      "Secure RAM access from Trusted world only"
      # Secure                                PASS
      # Non Secure                            PASS

```

The following is a snippet of a successful skip test on the display console.

```

----- Secure RAM Tests -----
121 : "R160/R180_TB_SA_INFRA"
      "Secure RAM access from Trusted world only"
      # Secure                                SKIP
      # Non Secure                            SKIP

```

This section contains the following subsection:

- [3.6.1 Debugging of a failing test on page 3-28.](#)

### 3.6.1 Debugging of a failing test

Since each test is organized with a logical set of self-checking code, searching for the relevant self-checking point during test failure is a useful point to start the debugging.

Consider this snippet of a failing test on the display console.

```

----- Trusted Boot Tests -----
21  : "R010/R020/R030/R090_TB_SA_BOOT"
      "Trusted boot operation from Trusted and Non-trusted world"
      # Secure
      Checkpoint C01 : Status = 8C
                                     FAIL
      # Non Secure
                                     FAIL

```

Here are some debugging points to consider.

1. This test is failing for the Trusted Boot component. Hence the test should be under `test_pool/boot/` directory.
2. The test ID is 21 which means it is the first test in the Trusted Boot component. Hence the test is `test_pool/boot/test_s001` directory.
3. Each test has a Secure and a Non-secure portion. In the above snippet, the failure is from the Secure portion. So you must see the `test_pool/boot/test_s001/secure.c` file.
4. Since the failure is shown as Checkpoint C01, the first checkpoint is failing with a status 8C.
5. The status of the failure is mapped with a structure `tbsa_status_t` that is available at `val/include/val_common.h`. In this example, 8C means that the test is failing for an incorrect value.

# Appendix A

## Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- [A.1 Revisions on page Appx-A-30.](#)

## A.1 Revisions

**Table A-1 Issue PJDOC-2042731200-3327**

Change	Location	Affects
This is the first revision of the document.	-	All revisions

**Table A-2 Differences between Issue PJDOC-2042731200-3327 and Issue 0000-01**

Change	Location	Affects
Updated directory structure.	See <a href="#">1.5.1 Directory structure on page 1-15</a> .	All revisions
Updated porting steps.	See <a href="#">Porting steps to create a new target</a> .	All revisions
Updated test naming conventions.	See <a href="#">3.5 Test naming conventions on page 3-27</a> .	All revisions

**Table A-3 Differences between Issue 0000-01 and Issue 0000-02**

Change	Location	Affects
Updated test naming conventions table.	See <a href="#">3.5 Test naming conventions on page 3-27</a>	All revisions.
Updated PAL APIs.	See <a href="#">PAL APIs</a>	All revisions.

**Table A-4 Differences between Issue 0000-02 and Issue 0000-03**

Change	Location	Affects
Updated the directory structure, software and tools, and memory requirements.	See <a href="#">1.5 Getting started on page 1-15</a> .	All revisions.
Updated the build steps and the build output directory structure.	See <a href="#">3.2 Build flow on page 3-22</a> .	All revisions.